Substitute for Form 1449 TO INFORMATION ISCLOSURE STATEMENT BY APPLICANT Sheet _1_ of _1_

Application No.	10/771,596
Filing Date	02/04/2004
First Named Inventor	Alfredo Herrera
Art Unit	2825
Examiner	V. SIEK
Attorney Docket No.	16550ROUS01U

U.S. PATENT DOCUMENTS						
Examiner's Initials	Citation Number	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document		
	A1					
	A2					
	A3					

	FOREIGN PATENT DOCUMENTS						
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	B1						
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OTHER PRIOR ART NON-PATENT LITERATURE DOCUMENTS			
Examiner's Initials	Citation Number	Document Description Include the name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	C1	Field Programmable Gate Arrays An Enabling Technology, (11 pages)	
	C2	S. Lorenzini, FPGA Design Cycle Time Reduction and Optimization, (2 pages)	
	C3	J. Ma, et al., Incremental Design Techniques for Million-Gate FPGAs, VTIP Disclosure No.: 01-110 (1 page)	
	C4	Xilinx Design Reuse Methodology for ASIC and FPGA Designers, (27 pages)	

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